The Portable Cell Libraries of the Freeware Alliance CAD system

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Abstract

The Freeware **Alliance** *CAD system is a set of technology independent libraries plus a set of tools dedicated to digital CMOS vlsi design.*
We present an overview of the functionalities available within the system libraries, including VHDL behavior, netlist and symbolic layout views for all cells. Both standard cells libraries and custom block generators are detailed, since it is a unique feature of **Alliance** *to provide such portable optimized generators.*
We'll also introduce the tools that, used in conjunction with the cells, will help to specify, develop and verify high complexity CMOS circuits.

1 Introduction

The manpower needed for the physical design of a cell library is extremely important. A given foundry may provide new CMOS processes every other year. The difficulty is even higher when multisourcing is to be achieved. In order to preserve the investment in library physical design, it is necessary to ensure that it can be used on different target technologies. Let's note that the overall digital CMOS **Alliance** portable libraries contains about 600 cells, either standard cells or parametrizable layout generator leaf cells. Four years have been needed for specification and development.
Portability constraints are different regarding the kind of cell library.

Standard cells libraries
Used in conjunction with place and route tools, all the cells must have the same height, share power supplies, and respect half design rules on right and left sides, for cell rows construction.

Parametrizable generators
The generators are designed using a *tiler and leaf cells* methodology. These leafs cells are dedicated to a given parametrizable generator. They have variable size, no specific strategy for power and ground, and have strong pitch matching constraints in both x and y direction with given neighbouring cells. The end user is expected to know only about a generated object, but not about the leaf cells it is based upon.

If these two types of libraries are of concern, as in the CMOS **Alliance** package, the technological mapping has to warranty the abutment properties. This is achieved by the fixed grid without compaction symbolic approach, as described in [1].
We will, in section2, give an overview of the functionalities provided by the **Alliance** portable libraries.
Section 3 will briefly review the **Alliance** CAD tools, that are the result of a ten years effort at the UPMC university in Paris.

2 Process independent cell libraries

The availability of CMOS cell libraries is limited. Either they contain proprietary optimized blocks, and the design has no technological migration possibility. Or the designer uses only standard cells, giving as a result poor chip performances in terms of density and speed.
The **Alliance** package provide a wide range of libraries, either static, ie fixed cells, or dynamic, as the block is produced by running a generator with fixed parameters.
Each object in the library has, for static ones, or produces, for dynamics ones, three views at least :

- the symbolic layout, that describes the cell topology.
- the netlist, in terms of transistor interconnections.
- the behavior, specified in VHDL data flow form.

A translation tool, taking as input the symbolic layout, performs the final process mapping to the target technology according to a technological file. The output is a hierarchical cif or GDSII file.
Area loss compared to micron design has been estimated ranging from 10% to 20%. But in fact, since the design is done only once, great care can be taken for both local and global optimization. Anyway, loosing area is affordable, where loosing years is not.

2.1 Standard cell libraries

Two kinds of "standard" libraries are available.
The *SCLIB* library contains boolean functions, buffers, mux, latches, flip-flops, . . . All the cells have the same height, share the power and ground lines on east and west side, and have pitched I/Os in metal2 on north and south side. They are supposed to be used with an usual standard cells place and route tool. These cells are to be used primary for glue logic, since optimized operators can be obtained using dedicated generators, as stated paragraph 2.2.
DPLIB is a cell library dedicated to high density data-paths. It must be used in conjunction with the data-path compiler **`fitpath`**[2]. Here the cells share the power and ground lines in metal2. A powerful dedicated over the cell router[3] can route custom blocks and logic glue in the same structure.
The figure 2.1 below shows the difference between *SCLIB* and *DPLIB* regarding the shape and contents of a cell.

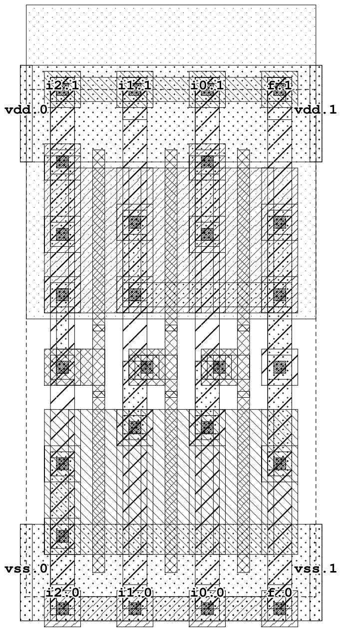

Figure 1: *SCLIB* version of a three inputs **`and`** gate

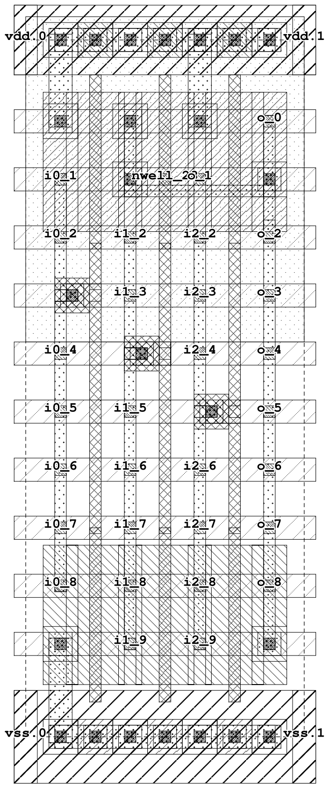

Figure 2: *DPLIB* version of a three inputs **`and`** gate

2.2 The custom block generators

Six optimized blocks generators are currently available in the **Alliance** package. Four of them have been designed to fit in the data-path structure used in the data-path compiler. The remaining two are parametrized *ROM* and *RAM* generators. All the generators are build with a tiler using a dedicated leaf cell library. Their output is a symbolic layout, a VHDL behavior, a set of pattern for test purpose, a netlist, an icon, and a datasheet indicating size and timing estimation for a given technology. The structural parameters varies according to their functionalities.

- Data-path oriented generators:

  `rsa`, a fast adder generator, with propagation time in log *nb* and size in *nb* log *nb*, where *nb* is the number of bits. Its has 2 or 3 input buses, and if needed a carry input. It may be used as a substractor or adder/substractor.

Parameters	Meaning	Range
nb	number of bits	3 to 128
cin	carry in	true or false
csa	three inputs adder	true or false
ovr	overflow flag	true or false

rfg, a static register file generator. It has one write address , and one or two read address. It may be operated as a set of level-sensitive latches or edge triggered flip-flops.

Parameters	Meaning	Range
nb	number of bits	2 to 64
nw	number of words	2 to 256
bus	number of read bus	1 or 2
op	mode of operation	latch or flip-flop
low power	reduce power consumption	true or false

bsg, a barrel shifter generator. Possible operations are :

- logical right shift
- arithmetical right shift
- logical left shift
- arithmetical left shift
- right rotation
- left rotation

Parameters	Meaning	Range
nb	number of bits	3 to 64

amg, an integer modified booth algorithm array multiplier. the x and y inputs are independent, and pipeline stages can be inserted in the circuit.

Parameters	Meaning	Range
nx	number of bits of the x operand	8 to 64
ny	number of bits of the y operand	8 to 64
ps	number of pipeline stages to be inserted in the circuit	0 to min($\frac{nx}{2}$, $\frac{ny}{2}$)-1

- *ROM* and *RAM* generators:

grog, a generic *ROM* generator. The interface is an address bus, a clock and an output enable signal, and a data out bus. The coding format to specify the *ROM* contents is a limited subset of VHDL.

Parameters	Meaning	Range
nb	number of bits	1 to 64
nw	number of words	64, 128, 256, n 512, $1 \leq n \leq 8$
hz	tri-state output	true or false

rage, a *RAM* generator. The interface has a read/write address, a write signal indicating if a read or a write is to be performed, and a clock.

Parameters	Meaning	Range
nb	number of bits	2 to 128
nw	number of words	128 to 4096
aspect	aspect ratio	narrow, medium or large
ud	unidirectional, ie share the same bus for data in and out	true or false

All these generators have been designed using the **Alliance** CAD tools, for both design and verification phases.

3 Alliance Tools overview

All the **Alliance** tools read their input and write their output through shared object oriented canonical data structures. This ensure interoperability between tools, thanks to a fixed semantic for each object in the data structure. Therefore, Over 1000 pages of documentation are available to the CAD tool developer in **unix man** format.
The **Alliance** tools organization around the three basic views of *vlsi* design is shown figure 3.
A short description of the available **Alliance** tools is given below:

asimut is a native VHDL logic simulator. The supported VHDL subset allows structural and behavioral data-flow zero delay description. Complex microprocessors including **Motorola** 6800 and **dlx** have been successfully modelizated and simulated using **asimut**.

genpat is a language interpreter dedicated to efficient simulation patterns descriptions to be taken as input of **asimut**. These patterns can be translated to MSA format for the Tektronix LV500 tester.

logic is a logic synthesis tool. The input is data-flow VHDL, the output is a netlist of gates. **logic** result can be mapped on any standard cell library as long as a VHDL description is provided with each cell. **logic** can also run without a predefined library, thanks to an internal CMOS standard cell compiler.

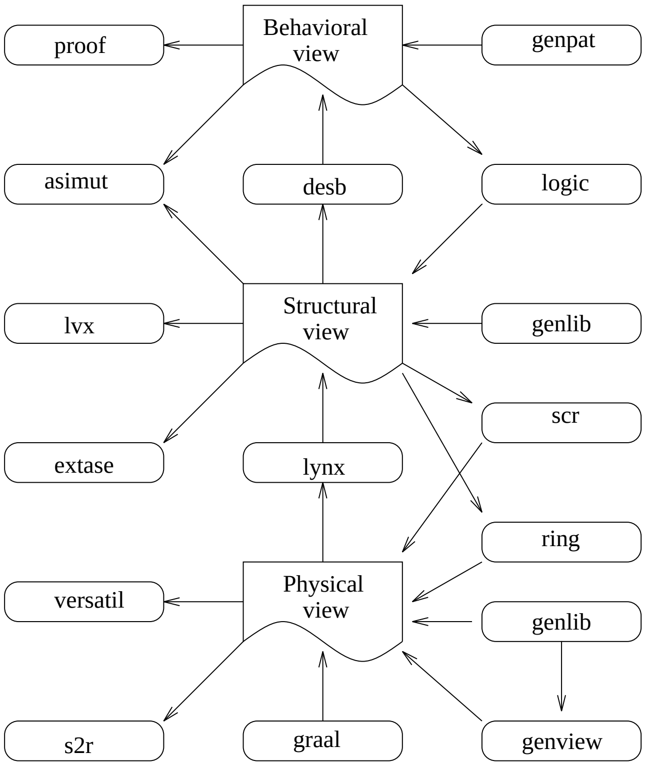

Figure 3: Basic views and tools.

genlib is a procedural language for netlist capture and placement description. It is a superset of the **C** language, with dedicated primitives for netlist and chip assembling. **genlib** is actually used to build parametrized generators.

genview is a **genlib** plus **C** graphical sources level debugger. Step by step execution and tiling result visualization is to be done under a standard X11 environment[4].

scr is a place and route tool for standard cells. Placement is based on simulated anealing. Feed throughs are automatically inserted where needed while routing.

ring is a core to pad router, making the final chip assembly between a rectangular core and the input/output pads. Pad placement optimization and supplies distribution are taken into account.

versatil is a design rule checker. It checks a possibly hierarchical symbolic layout. **versatil** uses a windowing algorithm to enhance performances.

lynx is a layout extractor. The input is a possibly hierarchical symbolic layout. The output is an extracted netlist with parasitic capacitances.

lvx is a gate level net compare tool. The result indicates whether or not the two input netlists are identical.

desb is a functional abstractor disassembler for CMOS circuits[5]. It provides a data flow VHDL description from a transistor netlist of a circuit. **desb** can be distinguished from commercial CAD abstractor by the fact that it does not require a predefined cell library.

proof performs a formal comparison between two data flow VHDL description. **proof** supports the same subset of VHDL as **asimut**, **logic**, and **desb**.

extase is a timing analyser. The input is an extracted netlist with capacitance. The tool allows simple interpretation under a **X11-Motif** environment of static timing analysis complex results[6].

graal is a hierarchical symbolic layout editor. It requires the **XWindows** plus **Motif** graphical environment. **graal** provides on line DRC and automatic display of equipotential nets.

s2r is the last tool of the methodology. **s2r** stands for Symbolic to Real, as the tool translate a hierarchical symbolic layout into physical layout required by a given silicon fabrication line, by the mean of a parametrizable technology file. Output formats are either CIF or GDSII.

4 Results and conclusion

Alliance has been successfully used for over three years, as practical support for undergraduate course on vlsi design and post graduate projects. The projects range from medium complexity ASICs to high complexity microprocessors.

Project	Number of transistors	Functionality
smal	17000	one bit processor for SIMD architectures
data safe	35000	dynamic data encryption chip
tnt	60000	switch router for T800 transputers
dlxm	28000	the dlx-m microprocessor as described in [7]
frisc	200000	floating point RISC microprocessor
stacs	800000	static control superscalar microprocessor

The overall contents of the **Alliance** CAD system is:

- over 150 documented standard cells for standard cell or data-path design.
- Six custom highly optimized documented generators, based upon 450 undocumented leaf cells, that can generated thousands of differents optimized blocks.
- three views, behavior, netlist and symbolic layout representation, for each cell.

The **Alliance** CAD system is freely available on anonymous ftp at **`cao-vlsi.ibp.fr`**.

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